WHAT IS CLAIMED IS:

1. A system for designing a configurable processor, the system comprising:

means for, based on a configuration specification, generating a description of a hardware implementation of the processor; and

means for, based on the configuration specification, generating software development tools specific to the hardware implementation.

2. The system of claim 1, wherein the means for generating software development tools comprises means for generating software development tools capable of generating code to run on the processor.

3. The system of claim 1, wherein the software development tools include a compiler, tailored to the configuration specification, for compiling an application into code executable by the processor.

4. The system of claim 1, wherein the software development tools include an assembler, tailored to the configuration specification, for assembling an application into code executable by the processor.

5. The system of claim 1, wherein the software development tools include a linker, tailored to the configuration specification, for linking code executable by the processor.

6. The system of claim 1, wherein the software development tools include a disassembler, tailored to the configuration specification, for disassembling code executable by the processor.

7. The system of claim 1, wherein the software development tools include a debugger, tailored to the configuration specification, for debugging code executable by the processor.

8. The system of claim 7, wherein the debugger has a common interface and configuration for instruction set simulator and hardware implementations.

9. The system of claim 1, wherein the software development tools include an instruction set simulator, tailored to the configuration specification, for simulating code executable by the processor.

10. The system of claim 9, wherein the instruction set simulator is capable of modeling execution of code being simulated to measure key performance criteria including cycles of execution.

11. The system of claim 10, wherein the performance criteria are based on specific configurable microarchitectural features.

12. The system of claim 10, wherein the instruction set simulator is capable of profiling execution of the program being simulated to record standard profiling statistics, including a number of cycles executed in each simulated function.

13. The system of claim 1, wherein the hardware implementation description includes a detailed HDL hardware implementation description.

14. The system of claim 1, wherein the hardware implementation description includes synthesis scripts.

15. The system of claim 1, wherein the hardware implementation description includes place and route scripts.

16. The system of claim 1, wherein the hardware implementation description includes programmable logic device scripts.

17. The system of claim 1, wherein the hardware implementation description includes a test bench.

18. The system of claim 1, wherein the hardware implementation description includes diagnostic tests for verification.

19. The system of claim 1, wherein the hardware implementation description includes scripts for running diagnostic tests on a simulator.

20. The system of claim 1, wherein the hardware implementation description includes test tools.

21. The system of claim 1, wherein the means for generating the hardware implementation description comprises:

means for generating a hardware description language description of the hardware implementation description from the configuration specification;

means for synthesizing logic for the hardware implementation based on the hardware description language description; and

means for placing and routing components on a chip based on the synthesized logic to form a circuit.

22. The system of claim 21, the means for generating the hardware implementation description further comprising:

means for verifying timing of the circuit; and

means for determining the area, cycle time and power dissipation of the circuit.

23. The system of claim 1, further comprising means for generating the configuration specification.

24. The system of claim 23, wherein the means for generating the configuration specification is responsive to selection of configuration parameters by a user.

25. The system of claim 23, wherein the means for generating the configuration specification is for generating the specification based on design goals for the processor.

26. The system of claim 1, wherein the configuration specification includes at least one parameter specification of a modifiable characteristic of the processor.

27. The system of claim 26, wherein the at least one parameter specification specifies the inclusion of a functional unit, and at least one processor instruction operating the functional unit.

28. The system of claim 27, wherein the functional unit is a multiplier and the parameter specification specifies at least one multiply instruction operating the multiplier.

29. The system of claim 27, wherein the functional unit is a multiply-accumulate unit and the parameter specification specifies at least one instruction performing a compound multiply, accumulate, operand load and address update operation.

30. The system of claim 27, wherein the functional unit is a digital signal processor and the parameter specification specifies at least one instruction operating the digital signal processor.

31. The system of claim 27, wherein the functional unit is a coprocessor and the parameter specification specifies at least one instruction operating the coprocessor.

32. The system of claim 26, wherein the at least one parameter specification specifies one of the inclusion, exclusion and features of a structure affecting processor state.

33. The system of claim 32, wherein the structure is a register file and the parameter specification specifies the number of registers in the register file.

34. The system of claim 32, wherein the structure is an instruction cache.

35. The system of claim 34, wherein the parameter specification specifies the size of the cache.

36. The system of claim 35, wherein the parameter specification specifies the line size of the cache.

37. The system of claim 35, wherein the parameter specification specifies set associativity of the cache.

38. The system of claim 32, wherein the structure is a data cache.

39. The system of claim 38, wherein the parameter specification specifies the size of the cache.

40. The system of claim 38, wherein the parameter specification specifies the line size of the cache.

41. The system of claim 38, wherein the parameter specification specifies the set associativity of the cache.

42. The system of claim 32, wherein the structure is a write buffer.

43. The system of claim 32, wherein the structure is one of an on-chip ROM and an on-chip RAM.

44. The system of claim 26, wherein the at least one parameter specification specifies a semantic characteristic controlling the interpretation of at least one of data and instructions in the processor.

45. The system of claim 44, wherein the semantic characteristic is instruction byte ordering and the parameter specification specifies one of big endian and little endian byte ordering.

46. The system of claim 44, wherein the semantic characteristic is a code density of the instruction set.

47. The system of claim 26, wherein the at least one parameter specification specifies an execution characteristic controlling the execution of instructions in the processor.

48. The system of claim 47, wherein the execution characteristic is the number of external interrupts of the processor.

49. The system of claim 47, wherein the execution characteristic is the number of interrupt priority levels of the processor.

50. The system of claim 47, wherein the execution characteristic is the number of interrupt timers of the processor.

51. The system of claim 47, wherein the execution characteristic is that a cache is one of a write-back cache and a write-through cache.

52. The system of claim 47, wherein the execution characteristic is synchronization of the processor with another processor.

53. The system of claim 47, wherein the execution characteristic is software-controlled branch speculation.

54. The system of claim 47, wherein the execution characteristic is a windowing operation of processor registers.

55. The system of claim 26, wherein the at least one parameter specification specifies debugging characteristics of the processor.

56. The system of claim 55, wherein the debugging characteristics include one of the inclusion and exclusion of an address trace and pipeline port.

57. The system of claim 55, wherein the debugging characteristics include one of the inclusion and exclusion of instruction and data break point support.

58. The system of claim 55, wherein the debugging characteristics include verification support.

59. The system of claim 26, wherein the configuration specification includes a parameter specification specifying at least one of a selection of a predetermined feature; a size or number of a processor element; and an assignment of a value.

60. The system of claim 1, further comprising means for evaluating suitability of the configuration specification.

61. The system of claim 60, wherein the means for evaluating includes an interactive estimation tool.

62. The system of claim 60, wherein the means for evaluating is for evaluating hardware characteristics of a processor described by the configuration specification.

63. The system of claim 60, wherein the means for evaluating is for evaluating the suitability of the configuration specification based on estimated performance characteristics of the processor.

64. The system of claim 63, further comprising means for providing information enabling modification of the configuration specification based on the estimated performance characteristics.

65. The system of claim 63, wherein the performance characteristics include at least one of area required to implement the processor on a chip, power consumed by the processor and clock speed of the processor.

66. The system of claim 60, wherein the means for evaluating is for evaluating suitability of the configuration specification based on estimated software characteristics of the processor.

67. The system of claim 66, wherein the means for evaluating is for presenting a suitability evaluation to a user interactively by estimating at least one of code size and cycles required to execute a suite of benchmark programs on a processor described by the configuration specification.

68. The system of claim 60, wherein the means for evaluating is for evaluating hardware characteristics and software characteristics of a processor described by the configuration specification.

69. The system of claim 1 wherein the means for generating is further for providing a characterization of hardware performance and cost and software application performance together to facilitate modification the configuration specification.

70. The system of claim 1 wherein the means for generating is further for providing a characterization of hardware performance and cost and software application performance together to facilitate an extension of the configuration specification.

71. The system of claim 1 wherein the means for generating is further for providing a characterization of hardware performance and cost and software application performance together to facilitate modification of the configuration specification, and for providing a characterization of hardware performance and cost and software application performance together to facilitate the description of an extension of the configuration specification.

72. The system of claim 1, further comprising means for generating a configuration of the processor by extension.

73. The system of claim 1, wherein the configuration specification includes at least one extension specification of an extensible characteristic of the processor.

74. The system of claim 73, wherein the extension specification specifies an additional instruction.

75. The system of claim 73, wherein the extension specification specifies inclusion of a user-defined instruction and an implementation for the instruction.

76. The system of claim 75, wherein the means for generating the software development tools includes means for suggesting to the user potential user-defined instructions particularly suited to at least one application.

77. The system of claim 75, wherein the software development tools include a compiler capable of generating the user-defined instruction.

78. The system of claim 77, wherein the compiler is capable of optimizing code containing user-defined instructions.

79. The system of claim 75, wherein the software development tools include an assembler capable of generating the user-defined instruction.

80. The system of claim 75, wherein the software development tools include a simulator capable of simulating execution of user code using the user-defined instruction.

81. The system of claim 75, wherein the software development tools include tools capable of verifying the user implementation of the user-defined instruction.

82. The system of claim 74, wherein the compiler is capable of automatically generating additional instructions.

83. The system of claim 73, wherein:

the extension specification specifies a new feature having functionality substantially designed by a user in abstract form; and

the means for generating the hardware implementation description is further for redefining and integrating the new feature into the detailed hardware implementation description.

84. The system of claim 83, wherein the extension specification is a statement in an instruction set architecture language specifying an opcode assignment and an instruction semantic.

85. The system of claim 84, wherein the means for generating the hardware implementation description includes means for generating instruction decode logic from the instruction set architecture language definition.

86. The system of claim 85, wherein the means for generating the hardware implementation description further includes means for generating signals specifying register operand usage for instruction interlock and stall logic based on the instruction set architecture language definition.

87. The system of claim 83, wherein the means for generating software development tools includes means for generating an instruction decode process used in an instruction set simulator tailored to the configuration specification.

88. The system of claim 83, wherein the means for generating software development tools includes means for generating encode tables used in an assembler tailored to the configuration specification.

89. The system of claim 83, wherein the means for generating the hardware implementation description is further for generating a description of datapath hardware for the new feature, the datapath hardware being consistent with a particular pipelined architecture of the processor.

90. The system of claim 73, wherein the additional instruction adds no new state to the processor.

91. The system of claim 73, wherein the additional instruction adds state to the processor.

92. The system of claim 1, wherein the configuration specification includes at least a portion specified by an instruction set architecture description language description.

93. The system of claim 92,wherein the means for generating the hardware implementation description comprises means for generating instruction decode logic automatically from the instruction set architecture language description.

94. The system of claim 92, wherein the means for generating software development tools comprises means for generating an assembler core automatically from the instruction set architecture language description.

95. The system of claim 92, wherein the means for generating software development tools comprises means for generating a compiler automatically from the instruction set architecture language description.

96. The system of claim 92, wherein the means for generating software development tools comprises means for generating a disassembler automatically from the instruction set architecture language description.

97. The system of claim 92, wherein the means for generating software development tools comprises means for generating an instruction set simulator automatically from the instruction set architecture language description.

98. The system of claim 1, wherein the means for generating the hardware implementation description includes means for preprocessing a portion of at least one of the hardware implementation description and the software development tools to modify the hardware implementation description and the software tools, respectively, based on the configuration specification.

99. The system of claim 98, wherein the means for preprocessing is for evaluating an expression in one of the hardware implementation description and the software development tools and replacing the expression with a value based on the configuration specification.

100. The system of claim 99, where the expression includes at least one of an iterative construct, a conditional construct and a database query.

101. The system of claim 1, wherein the configuration specification includes at least one parameter specification specifying a modifiable characteristic of the processor and at least one extension specification specifying an extensible characteristic of the processor.

102. The system of claim 101, wherein the modifiable characteristic is one of a modification to the core specification and an optional feature not specified in the core specification.

103. The system of claim 1, wherein the configuration specification includes at least one parameter specification specifying a binary selectable characteristic of the processor, at least one parametrically specifiable characteristic of the processor, and at least one extension specification specifying an extensible characteristic of the processor.

104. A method of designing a configurable processor, the method comprising:

generating a description of a hardware implementation of the processor based on a configuration specification; and

generating software development tools specific to the hardware implementation based on the configuration specification.

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